

We claim:

1. A method of forming a substrate for use in IC device fabrication comprising:

preparing a silicon substrate, including doping a bulk silicon (100) substrate with

ions taken from the group of ions to form a doped substrate taken from the group of doped

5 substrates consisting of n-type doped substrates and p-type doped substrates;

forming a first relaxed SiGe layer on the silicon substrate;

forming a first tensile-strained silicon cap on the first relaxed SiGe layer;

forming a second relaxed SiGe layer on the first tensile-strained silicon cap;

forming a second tensile-strained silicon cap on the second relaxed SiGe layer; and

10 completing an IC device.

2. The method of claim 1 wherein the IC device is a CMOS device, and wherein said

completing includes completing a CMOS device on the tensile-strained silicon cap, wherein the

CMOS device includes a source region and a drain region which are both in electrical contact with

15 a tensile-strained silicon cap, including well ion implantation, threshold voltage adjustment, STI

device isolation, gate oxidation, gate electrode and sidewall nitride formation; etching of gate

oxide after formation of sidewall nitride; etching of exposed second tensile-strained silicon cap to

expose second relaxed SiGe layer in the source region and the drain region; selectively laterally

etching of any SiGe layer at the source and drain region and selectively laterally etching of any

20 SiGe layer located beneath the gate and nitride spacers, forming a resulting tunnel, which is left  
empty or filled with a dielectric.

3. The method of claim 1 wherein said forming a first relaxed SiGe layer on the silicon substrate includes forming a graded, relaxed SiGe layer to a thickness of between about 200 nm to 5  $\mu$ m, and containing between about 10% and 100% Ge, and preferably between about 20% to 30% Ge.

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4. The method of claim 1 wherein said forming a first tensile-strained silicon cap includes forming a tensile-strained silicon cap to a thickness of between about 10 nm to 50 nm.

5. The method of claim 1 wherein said forming a second relaxed SiGe layer on the silicon substrate includes forming a relaxed SiGe layer to a thickness of between about 25 nm to 300 nm.

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6. The method of claim 1 wherein said forming a second tensile-strained silicon cap includes forming a second tensile-strained silicon cap having a thickness of between about 10 nm to 50 nm.

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7. A method of forming a substrate for use in CMOS fabrication comprising:  
preparing a silicon substrate, including doping a bulk silicon (100) substrate with  
ions taken from the group of ions to form a doped substrate taken from the group of doped  
substrates consisting of n-type doped substrates and p-type doped substrates;

5 forming a first relaxed SiGe layer on the silicon substrate;  
forming a first tensile-strained silicon cap on the first relaxed SiGe layer; and  
completing a CMOS device on the tensile-strained silicon cap, wherein the CMOS  
device includes a source region and a drain region which are both in electrical contact with a  
tensile-strained silicon cap.

10 8. The method of claim 7 wherein said forming a first relaxed SiGe layer on the  
silicon substrate includes forming a relaxed SiGe layer to a thickness of between about 200 nm to  
5  $\mu\text{m}$ .

15 9. The method of claim 7 wherein said forming a first relaxed SiGe layer on the  
silicon substrate includes forming a graded relaxed SiGe layer, containing between about 10% and  
100% Ge, and preferably between about 20% to 30% Ge.

10. The method of claim 7 wherein said forming a first tensile-strained silicon cap  
20 includes forming a tensile-strained silicon cap to a thickness of between about 10 nm to 50 nm.

11. The method of claim 7 which includes forming a second relaxed SiGe layer on the first tensile-strained silicon cap and forming a second tensile-strained silicon cap on the second relaxed SiGe layer.

5 12. The method of claim 11 wherein said forming a second relaxed SiGe layer on the silicon substrate includes forming a relaxed SiGe layer to a thickness of between about 25 nm to 300 nm.

13. The method of claim 11 wherein said forming a second tensile-strained silicon cap  
10 includes forming a second tensile-strained silicon cap having a thickness of between about 10 nm to 50 nm.

14. The method of claim 11 wherein said completing a CMOS device on the tensile-strained silicon cap, wherein the CMOS device includes a source region and a drain region which  
15 are both in electrical contact with a tensile-strained silicon cap, includes well ion implantation, threshold voltage adjustment, STI device isolation, gate oxidation, gate electrode and sidewall nitride formation; etching of gate oxide after formation of sidewall nitride; etching of exposed second tensile-strained silicon cap to expose second relaxed SiGe layer in the source region and the drain region; selectively laterally etching of any SiGe layer at the source and drain region and  
20 selectively laterally etching of any SiGe layer located beneath the gate and nitride spacers, forming a resulting tunnel, which is left empty or filled with a dielectric.

15. The method of claim 11 wherein said completing a CMOS device on the tensile-strained silicon cap, wherein the CMOS device includes a source region and a drain region which are both in electrical contact with a tensile-strained silicon cap, includes well ion implantation, threshold voltage adjustment, STI device isolation, gate oxidation, gate electrode and sidewall  
5 nitride formation; etching of gate oxide after formation of sidewall nitride; etching of exposed second tensile-strained silicon cap to expose second relaxed SiGe layer in the source region and the drain region; selectively laterally etching of any SiGe layer at the source and drain region and selectively laterally etching of any SiGe layer located beneath the gate and nitride spacers, forming a resulting tunnel, which is left empty or filled with a dielectric.

16. A method of forming a substrate for use in CMOS fabrication comprising:  
preparing a silicon substrate, including doping a bulk silicon (100) substrate with ions taken from the group of ions to form a doped substrate taken from the group of doped substrates consisting of n-type doped substrates and p-type doped substrates;

5 forming a first relaxed SiGe layer on the silicon substrate, including forming a graded, relaxed SiGe layer to a thickness of between about 200 nm to 5  $\mu$ m, and containing between about 10% and 100% Ge, and preferably between about 20% to 30% Ge;

forming a first tensile-strained silicon cap on the first relaxed SiGe layer having a thickness of between about 10 nm to 50 nm; and

10 completing a CMOS device on the tensile-strained silicon cap, wherein the CMOS device includes a source region and a drain region which are both in electrical contact with a tensile-strained silicon cap.

17. The method of claim 16 which includes forming a second relaxed SiGe layer on the first tensile-strained silicon cap and forming a second tensile-strained silicon cap on the second relaxed SiGe layer.

18. The method of claim 17 wherein said forming a second relaxed SiGe layer on the silicon substrate includes forming a relaxed SiGe layer to a thickness of between about 25 nm to 300 nm.

19. The method of claim 17 wherein said forming a second tensile-strained silicon cap includes forming a second tensile-strained silicon cap having a thickness of between about 10 nm to 50 nm.

5 20. The method of claim 17 wherein said completing a CMOS device on the tensile-strained silicon cap, wherein the CMOS device includes a source region and a drain region which are both in electrical contact with a tensile-strained silicon cap, includes well ion implantation, threshold voltage adjustment, STI device isolation, gate oxidation, gate electrode and sidewall nitride formation; etching of gate oxide after formation of sidewall nitride; etching of exposed  
10 second tensile-strained silicon cap to expose second relaxed SiGe layer in the source region and the drain region; selectively laterally etching of any SiGe layer at the source and drain region and selectively laterally etching of any SiGe layer located beneath the gate and nitride spacers, forming a resulting tunnel, which is left empty or filled with a dielectric.

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21. The method of claim 16 wherein said completing a CMOS device on the tensile-strained silicon cap, wherein the CMOS device includes a source region and a drain region which are both in electrical contact with a tensile-strained silicon cap, includes well ion implantation, threshold voltage adjustment, STI device isolation, gate oxidation, gate electrode and sidewall  
5 nitride formation; etching of gate oxide after formation of sidewall nitride; etching of exposed second tensile-strained silicon cap to expose second relaxed SiGe layer in the source region and the drain region; selectively laterally etching of any SiGe layer at the source and drain region and selectively laterally etching of any SiGe layer located beneath the gate and nitride spacers, forming a resulting tunnel, which is left empty or filled with a dielectric.

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